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REMARKS

Reconsideration of the application is respectfully requested.

With regard to the indefiniteness rejection of claim 9, Applicants have described their "IP-based approach," for example, on pages 11, line 6 through page 13, line 15 of the present application. In that regard, the configuration memory of a programmable logic device may be configured to practice the logic flow illustrated and discussed with regard to Figure 3. Thus, Applicants have made it quite clear how the checksum calculation engine and the checksum comparator are "implemented" by appropriate configuration of the configuration memory. Accordingly, claim 9 is plainly definite.

With regard to the obviousness rejections of claim 1 – 24 over Plants (USP 6,237,124) in view of Carmichael (USP 7,036,059), Applicants have amended claim 1 to recite the following inventive feature discussed, for example, on page 9, lines 1 through 6 of the present application. In this aspect of the invention, the configuration memory cells storing a LUT-based logic block's truth table may instead be used as random access memory (RAM). Because the contents of RAM may change during normal operation, each logic block may be associated with a status indicator indicating whether its configuration memory cells are being used as RAM. If a logic block's status indicator indicates its configuration memory cells are used as RAM, these cells are not included in the checksum calculation. Claim 1 reflects these advantageous features by including the limitation of "the checksum calculation excluding configuration data for logic blocks whose respective status indicator indicates the logic block is configured as random access memory."

The Plants reference is entirely silent regarding this innovation with regard to a logic block's status as RAM. The Carmichael reference adds nothing further. Accordingly, claim 1 and its dependent claims are allowable over the cited prior art.

Independent claims 11 and 15 have been amended analogously as discussed with regard to claim 1. Thus, these claims and their dependent claims are also allowable over the cited prior art.

New claim 25 is directed to the feature discussed, for example, on page 13, lines 20 – 23 wherein the programmable logic device includes a non-volatile memory storing the configuration data such that if the checksum calculation indicates an error, the

programmable logic device is re-configured using configuration data retrieved from the non-volatile memory.

New claim 26 limits the status indicator to comprise a status bit as discussed for example, on page 9, line 4.

New claim 27 limits the status indicator to comprise an address as discussed for example on page 9, lines 7 – 15.

New claim 28 is similar to claim 27, but excludes from the checksum calculation a logic block or a memory block whose address is stored with the configuration data in the configuration memory.

Claims 4, 8, 14, 18, and 21 – 24 are cancelled.

In addition, some minor typographical errors in the specification have been addressed.

For the foregoing reasons, Applicants respectfully submit that the pending claims are in proper form for allowance. Reconsideration and withdrawal of the rejections are respectfully requested and a timely Notice of Allowance is solicited.

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I hereby certify that this correspondence is being facsimile transmitted to the United States Patent and Trademark Office on the date shown below.

Tina Kavanaugh 9/5/2006

Tina Kavanaugh Date of Signature

Respectfully submitted,

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